CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER

Inventors: Jan Mulder
                    Yee Ling Cheung

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001]   This application is a Continuation of U.S. Patent Application No. 10/158,193, Filed: May 31, 2002, Titled: CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER, inventors: Mulder et al., which is a Continuation-in-Part of Application No. 10/153,709, Filed: May 24, 2002, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER et al.; and is related to Application No. 10/158,774, Filed: May 31, 2002; Titled: ANALOG TO DIGITAL CONVERTER WITH INTERPOLATION OF REFERENCE LADDER, Inventors: MULDER et al.; Application No. 10/158,595, Filed: May 31, 2002, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan MULDER; and Application No. 10/158,773, Filed: May 31, 2002, Inventor: Jan MULDER; Titled: SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING, Inventors: van der GOES et al., all of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002]   The present invention relates to line drivers, and more particularly to high-speed, low-distortion line drivers.

Related Art

[0003]   FIG. 1 shows a conventional output driver cell of a line driver currently employed in (Gigabit) Ethernet products. Each cell includes two differential pairs, enabling tri-state operation. Transistors **M1a** through **M1d** are cascodes, implemented using thick-oxide transistors. Transistors **M3a** and **M3b** implement the tail current sources of the two differential pairs, each

providing a current I_{BIAS}. Transistors **M2a** through **M2d** are switches (typically thin-oxide transistors) that control to which output terminal the bias current I_{BIAS} is sent. More specifically, when $V_{switch1}$ and $V_{switch3}$ are logical "1", and $V_{switch2}$ and $V_{switch4}$ are "0", the differential output current I_{OUT} equals -2 I_{BIAS}. When $V_{switch1}$ and $V_{switch3}$ are "0", and $V_{switch2}$ and $V_{switch4}$ are "1", I_{OUT} equals 2 I_{BIAS}. When $V_{switch1}$ through $V_{switch4}$ are all "1", I_{OUT} equals zero. (In other words, the digital signal, or data signal, activates the switching transistors **M2a-M2d**.) A more detailed description of a conventional line driver can be found in commonly assigned US Patent No. 6,259,745.

[0004] V_{BIAS} is a DC bias voltage that biases the tail current transistors **M3a**, **M3b** to an analog amplifier mode. The switches **M2a** - **M2d** send current to either the "+" or the "-" terminal of the output cell, which is a tri-state operating cell. The cell outputs either $2I_{BIAS}$, 0, or $-2I_{BIAS}$. To output zero current, while operating the cell in class B mode, gates of switches **M2a** - **M2d** are switched to ground, and no current appears at the output. Due to the charge injected at node ①, the potential at the gate of **M3** changes, resulting in distortion. Thus, there is unwanted modulation of the DC bias on the gate of the tail current transistors **M3a**, **M3b**.

[0005]   As noted above, when I_{OUT} has to be zero, $V_{switch1}$ through $V_{switch4}$ switch to "0". Unfortunately, switching off all four switches **M2a-M2d** results in significant distortion of the output signal I_{OUT}. The cause of the distortion is explained by **FIG. 2**, which shows half of a line driver output cell. The distortion occurs when all four switches **M2a-M2d** are switched to "0". In that case, node ② goes to ground potential. Through the parasitic capacitance C_p, charge is injected onto node ①. In general, the bias voltage V_{BIAS} is generated by a current-biased diode, which has a finite output impedance modeled by R_{BIAS}. Furthermore, the parasitic capacitance $C_{p,bias}$ associated with the bias voltage V_{BIAS} source and transistor **M3** is quite large. As a consequence, the charge injected onto node ① causes the voltage on node ① to drop. It settles back slowly due to the finite voltage source impedance and the large parasitic capacitance connected to node ①. This results in modulation of the tail

currents of the differential pairs, and therefore, in modulation of the amplitude of I_{OUT}, in other words, unwanted distortion.

[0006] I_{OUT} (in differential mode) = I_{OUT+} - I_{OUT-}. I_{OUT} is the differential output signal current. Its magnitude depends on the symbol to be transmitted and varies from –40mA to 40mA (in 1000BT, 100TX mode), from –100mA to 100 mA in 10BT mode). In Class AB mode, I_{COMMON_MODE} = $(I_{OUT+}$ - $I_{OUT-})/2$ varies from 20mA to 10mA, depending on the symbol to be transmitted. Thus: I_{COMMON_MODE} = 20 mA (in Class-A mode).

[0007] I_{COMMON_MODE} varies from 20 mA to 10 mA (in Class-AB mode), hence the maximum saving of current is 10 mA. When I_{COMMON_MODE} switches from 20 mA to 10 mA, a glitch is seen that eventually settles to constant value – i.e., producing unwanted distortion.

SUMMARY OF THE INVENTION

[0008] The present invention is directed to a line driver that substantially obviates one or more of the problems and disadvantages of the related art.

[0009] There is provided a differential line driver includes first, second, third and fourth cascode transistors connected in parallel, wherein drains of the first and third transistors are connected to a negative output of the differential line driver, and wherein drains of the second and fourth transistors are connected to a positive output of the differential line driver. First, second, third and fourth switching transistors are connected in series with corresponding the first, second, third and fourth cascode transistors and driven by a data signal. First and second compound transistors inputting a class AB operation signal at their gates, wherein the first compound transistor is connected to sources of the first and second switching transistors, and wherein the second compound transistor is connected to sources of the third and fourth switching transistors.

[0010] In another aspect of the present invention there is provided a differential line driver including first and second half-cells, the half-cells cross connected to positive and negative differential outputs, each half-cell

including first and second cascode transistors connected in parallel. First and second switching transistors are connected in series with the first and second cascode transistors and driven by a data signal. A first compound transistor inputs a class AB operation signal at its gate and connected to sources of the first and second switching transistors.

[0011]   In another aspect of the present invention there is provided a differential line driver includes first and second half-cells, the half-cells cross connected to positive and negative differential outputs, each half-cell including first and second cascode transistors are connected in parallel. First and second switching transistors are connected in series with the first and second cascode transistors and driven by a voltage. A tail current transistor inputs a bias voltage at its gate and connected to sources of the first and second switching transistors, wherein a sum of charge injection at the gate of the tail current transistor is substantially zero during switching.

[0012]   In another aspect of the present invention there is provided a class AB line driver including first and second half-cells cross connected to positive and negative differential outputs, each half-cell including first and second cascode transistors connected in parallel. First and second switching transistors are connected in series with the first and second cascode transistors. A tail current transistor inputs a bias voltage at its gate and connected to sources of the first and second switching transistors, wherein the bias voltage spikes last less than a clock cycle during switching for Gigabit Ethernet operation.

[0013]   In another aspect of the present invention there is provided a programmable line driver including a plurality of cells, each cell selectively controlled by class AB operation signal and each cell including first and second half-cells cross connected to outputs of opposite polarity, each half-cell including first and second parallel cascode transistors. First and second switching transistors are each connected in series with the first and second parallel cascode transistors. A compound transistor inputs a bias signal at its gate and connected to sources of the first and second switching transistors, the

compound transistor switched to class AB operation by the class AB operation signal, wherein same polarity outputs of the cells are added.

[0014]   In another aspect of the present invention there is provided a differential line driver including a plurality of cascode transistors connected in parallel and to corresponding polarity outputs of the differential line driver. A plurality of switching transistors are connected in series with corresponding cascode transistors. A plurality of compound transistors input a class AB operation signal at their gates and connected in series with corresponding switching transistors.

[0015]   In another aspect of the present invention there is provided a differential line driver including first and second half-cells, the half-cells cross connected to positive and negative differential outputs, each half-cell including first and second cascode transistors connected in parallel. First and second switching transistors connected in series with the first and second cascode transistors. A variable effective channel length transistor inputting a signal that changes its effective channel length at its gate and connected to sources of the first and second switching transistors.

[0016]   Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0017]   It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]   The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of

this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0019]   **FIG. 1** illustrates a conventional line driver;

[0020]   **FIG. 2** illustrates a half cell of a conventional line driver;

[0021]   **FIG. 3** illustrates a line driver of the present invention;

[0022]   **FIG. 4** illustrates a half cell of the line driver of the present invention;

[0023]   **FIG. 5** illustrates additional detail of the circuit of **FIG. 4**

[0024]   **FIG. 6** illustrates current and voltage waveforms at various nodes of **FIG. 5**;

[0025]   **FIG. 7** illustrates an output current waveform;

[0026]   **FIG. 8** illustrates a bias voltage waveform at node 1;

[0027]   **FIG. 9** illustrates a voltage waveform at node n3 of **FIG. 5**;

[0028]   **FIG. 10** illustrates a voltage waveform at nodes n3a and n3b of **FIG. 5**;

[0029]   **FIGs. 11** and **12** illustrate a multi-cell driver of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0030]   Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0031]   Low-power operation is very important for Gigabit Ethernet chips. The line driver is an important contributor to the overall power consumption. (The line driver, or transmitter, is frequently a digital-to-analog converter (DAC), but will be referred to as "line driver" herein.) Therefore, class AB or class B operation, instead of class A operation, are alternatives for decreasing the power consumption of the line driver.

[0032]   Line drivers frequently have class B operating mode. Unfortunately, the distortion of operating in that mode is higher than desired. A new circuit technique for implementing a low-distortion class AB line-driver for (Gigabit)

Ethernet applications, is described herein, allowing significant reduction in power consumption, while preserving sufficient line driver linearity. In order to reduce power consumption of the line driver, it is desirable to reduce the quiescent current (idle current) I_{IDLE}.

[0033]   Class A operation typically biases drivers to a certain (fairly large) quiescent current I_{IDLE}, e.g., I_{IDLE} = 40 mA. In class AB operation, the quiescent current I_{IDLE} is much smaller, or about 20 mA. For class B operation, the output cell is only turned on for when it is driving something, otherwise it is turned off. The idle current I_{IDLE} for class B operation is essentially zero. As noted above, I_{COMMON_MODE} = 10mA in class AB mode. Hence the I_{IDLE}--the output current during idle mode in the best case scenario-- is (10 mA + 10 mA) = 20 mA (10 mA from the positive terminal, 10 mA from the negative terminal) . In class A operation, I_{COMMON_MODE} = 20 mA and I_{IDLE}=40 mA (20 mA from the positive terminal, 20 mA from the negative terminal)

[0034]   The circuit of the invention prevents charge injection to node ① from occurring. To accomplish this, the simple tail current transistors **M3a**, **M3b** shown in FIG. 1 are replaced by "compound" transistors **301**, **302**, shown in FIG. 3. Transistors **M5a** and **M5b** are switches that control the effective channel length L_{EFF} of the compound transistors **301**, **302**. When $V_{\overline{CLASSAB}}$ is "0", L_{EFF} is determined by the channel length of the transistors **M3**, **M4** and **M6**. When $V_{\overline{CLASSAB}}$ is "1", **M5** effectively short circuits the transistor **M4**, and L_{EFF} is determined mainly by the channel length of the transistors **M3** and **M6**. Therefore, when $V_{\overline{CLASSAB}}$ switches from "1" to "0", L_{EFF} increases, which causes the tail current source, and hence the power consumption, to decrease. The output cell switches to class B operation when I_{OUT} needs to be zero, by switching $V_{switch1}$ through $V_{switch4}$ to "1" and $V_{\overline{CLASSAB}}$ to "0".

[0035]   Further with reference to FIG. 3, FIG. 3 shows a differential output cell, comprising two half-cells, a left half-cell and a right half-cell. The output

cell includes four cascode transistors M1a, M1b, M1c, and M1d, which are arranged in parallel. Drains of the cascode transistors M1a and M1c are connected to the negative polarity output, and drains of the cascode transistors M1b and M1d are connected to the positive polarity output of the differential cell. Gates of the cascode transistors M1a-M1d are driven by V_{CASC}. V_{CASC} is a DC voltage of approximately 1 volt, and output voltage is about 1.8 V in the idle state. The transistors M1a through M1d are implemented using thick-oxide transistors. Note that the drains of the transistors M1a-M1d are connected to a primary coil of a transformer (not shown in the figures). A center tap of the transformer is connected to a 1.8 V supply

[0036]   The four cascode transistors M1a-M1d are connected in series with corresponding switch transistors M2a-M2d, sources of the cascode transistors M1a-M1d connected in series with drains of the switch transistors M2a-M2d. Gates of the switch transistors M2a-M2d are driven by corresponding inputs $V_{switch1}$ through $V_{switch4}$. The transistors M2a through M2d are switches (typically thin-oxide transistors, driven by about 1-1.2 volts) that control to which output terminal the bias current I_{BIAS} is sent – i.e, a data signal drives the gates of the transistors M2a through M2d.

[0037]   Sources of the switch transistors M2a, M2b are tied together and to a "drain" of the compound transistor 301. The compound transistor 301 includes three internal transistors M3a, M4a, M6a connected in series. Gates of the internal transistors M3a, M4a, and M6a are connected to a bias voltage V_{BIAS}. The source of the last transistor, M6a, is connected to ground. A fourth internal transistor M5a is connected across M4a. A gate of the internal transistor M5a is driven by the $V_{\overline{CLASSAB}}$ signal. When the $V_{\overline{CLASSAB}}$ signal goes to a logical one, the transistor M4a is shorted, and the effective channel length L_{EFF} of the compound transistor 301 is reduced. The impedance of the transistor M5a is low when it is on.

[0038]   The compound transistor 302 operates in a similar manner to compound transistor 301.

[0039]   The table below shows the tri-state class AB operation of the circuit of **FIG. 3**:

M2a	M2b	M2c	M2d	output	$V_{\overline{CLASSAB}}$
0	1	0	1	I_{OUT+}	1
1	0	1	0	I_{OUT-}	1
1	1	1	1	I_{OUT+}, I_{OUT-}	0

[0040]   **FIG. 4** shows a half-cell of **FIG. 3**, with the parasitic capacitances shown as circuit elements. As shown on **FIG. 4**, node ① has $C_{P, bias}$, connected to ground (a bias parasitic capacitance). Parasitic capacitance C_{P1} is between node ① and node ②, parasitic capacitance C_{P2} is between node ① and node ③, and parasitic capacitance C_{P3} is between node ① and node ④.

[0041]   The transistors **M2a-M2d** are used as switches, and the compound transistors **301**, **302** are used as analog amplifiers. Typically, field effect transistors are used as the transistors illustrated in **FIG. 3**.

[0042]   The aspect ratios W/L of individual transistors comprising the compound transistor **301** (or **302**) are such that voltage at the node of V_{BIAS} (node ①) is not affected during switching, and idle current I_{IDLE} is reduced by about fifty percent. Because there are no substantial interruptions, or spiking of the bias voltage V_{BIAS}, the output current is much cleaner, and shows less distortion. Note that since $V_{\overline{CLASSAB}}$ changes the aspect ratio of the compound transistors **301**, **302**, instead of changing L_{EFF}, it is equally possible to change effective channel width, or both Leff and the effective channel width.

[0043]   Further with reference to **FIG. 4**, when the signal $V_{\overline{CLASSAB}}$ at the gate of **M5a** goes to zero, the potential at node ④ goes down, the potential at node ② goes up, and the potential at node ③ goes up. Thus, although more parasitics are involved, the net result of the charge injection is zero. C_{P1}, C_{P2}

and C_{P3} of **FIG. 4** deliver opposite polarity charges into node ①. Thus, although node ① has slow settling time, there is never any net charge injection, since the charge injection cancels out.

[0044]   The compound transistor **301** behaves as if it is a single transistor, even though in actuality it includes at least four transistors. The aspect ratio of the compound transistor **301** depends on the state of the switch **M5a**, since the effective channel length L_{EFF} varies depending on the input to **M5a**:

[0045]   Aspect Ratio= W/L_{EFF}

[0046]   By changing L_{EFF}, the effective aspect ratio W/L changes.

[0047]   Thus, **FIG. 4** explains why the new circuit implementation does not suffer from significant output current distortion. When the output cell switches to class-AB operation, the voltages on nodes ② and ③ will increase. Through parasitic capacitances C_{p1} and C_{p2} a positive charge injection onto node ① occurs. However, the voltage on node ④ will decrease and through C_{p3} a negative charge injection onto node ① occurs. If the dimensions of transistors **M3, M4, M6** are carefully chosen, the positive and negative charge injections cancel each other, leaving the voltage on node ① undisturbed. This enables low-distortion class AB operation.

[0048]   **FIG. 5** shows additional detail of the structure of the half-cell, including dimensions of transistors used in one embodiment of the present invention. For example, the transistor **M1a** has a width of 3.22 μm, and a length of 0.4 μm. The multiplicity factor m = 20 refers to the actual number of transistors **M1a** in each half-cell, i.e., in this case, 20. **FIG. 5** also shows four NMOS transistors MC2a, MC2b, MC1a, MC1b, whose sources and drains are connected to V_{SS}, so that they function as capacitors. With the transistors of **FIG. 5**, the aspect ratio is about **160** when $V_{\overline{CLASSAB}}$ is HIGH, and about 80 when $V_{\overline{CLASSAB}}$ is LOW. In other words, for **FIG. 5**, when $V_{\overline{CLASSAB}}$ is HIGH, the aspect ratio = 3.22 * 20 * 2 / (0.28 + 0.52) = 161.

[0049]   FIGs. 6 and 7 illustrate a simulation of the output current I_{OUT} of the present invention. As may be seen from FIGs. 6 and 7, the output current I_{OUT} is very clean, showing only a small spike upon transition when operating in Gigabit Ethernet and 100TX mode.

[0050]   FIG. 8 shows the potential at node ① (V_{BIAS1}), and particularly illustrating the small spike of approximately 20-25 mV upon transition. The three curves shown in FIG. 8 represent operation at three different temperatures, 125°C, SS process for the top curve, 75°C, TT process for the middle curve, and 25°C, FF process for the bottom curve. Here:

SS – slow NMOS transistor, slow PMOS transistor.

TT- typical NMOS transistor, typical PMOS transistor.

FF – fast NMOS transistor, fast PMOS transistor.

[0051]   As discussed above, such a small spike of 20-25 mV for a very short duration (i.e., substantially less than a clock cycle) results in a much cleaner output current, and very low distortion. Another way to look at it is to consider an area under the curve (i.e., spike energy) of each spike in FIG. 8, which is very low relative to overall pulse energy.

[0052]   FIG. 9 shows the voltage at node n3 of FIG. 5 at three different temperatures and processes, 125°C (SS process), 75°C (TT process), and 25°C (FF process). Similarly, FIG. 10 shows simulated voltages at nodes n3a and n3b of FIG. 5, at the three different temperatures discussed above. As may be seen from these figures, the voltage spikes on V_{BIAS} due to charge injection are very small, enabling low distortion operation.

[0053]   FIGs. 11 and 12 illustrates the entire line driver of the present invention that is comprised of a total of 40 output cells (24 cells are shown in FIG. 12) connected in parallel to each other, so that their output currents sum. Each "rectangle" in FIG. 12 corresponds to the circuit (cell) shown in FIG. 3. FIGs. 11 and 12 also illustrate that the output cells of the line driver can be grouped together so as to program their output current. For example, only the cells of Group 1 may be activated, resulting in an output current of 5 mA.

When all the groups are activated by $V_{\overline{CLASSAB}}$ being on, the total output current is 40 mA (i.e., 8 x 5 mA current of the single group).

[0054] Note that the 40 pair differential line driver can operate at 40 mA maximum output current at 1000 Base T mode, or TX mode, with 2 V_{PP} (peak to peak) output. It can also operate at 100 mA maximum output current in 10 Base T mode, 5 V_{PP} output.

[0055] The quiescent current I_{IDLE}, when in class AB operation, can be controlled in several different ways. First, the dimensions (aspect ratios) of the individual transistors that comprise the compound transistor, determine the quiescent current obtained within each output cell. Secondly, more elaborate compound transistors are possible that allow programmability of the quiescent current of the DAC output cells. Thirdly, the switches M5 of all output cells comprising the complete line driver do not have to be controlled by only one signal $V_{\overline{CLASSAB}}$. Using different switch signals (e.g., $V_{\overline{CLASSAB1}}$ ... $V_{\overline{CLASSAB8}}$) for different groups, or subsets, of output cells allows programmability of the overall quiescent current I_{IDLE} of the entire line driver.

[0056] The class AB line driver of the present invention can, in principle, be used in any application where a digital to analog converter (DAC) is used as a line driver.

[0057] It will be appreciated that the various aspects of the invention as further disclosed in U.S. Patent Application No. 10/158,193, Filed: May 31, 2002, Titled: CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER, inventors: Mulder et al.; Application No. 10/153,709, Filed: May 24, 2002, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER et al.; Application No. 10/158,774, Filed: May 31, 2002; Titled: ANALOG TO DIGITAL CONVERTER WITH INTERPOLATION OF REFERENCE LADDER, Inventors: MULDER et al.; Application No. 10/158,595, Filed: May 31, 2002, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan MULDER; and Application No. 10/158,773, Filed: May 31, 2002, Inventor: Jan MULDER; Titled: SUBRANGING ANALOG

TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING, Inventors: van der GOES et al., all of which are incorporated by reference herein, may be combined in various ways, or be integrated into a single integrated circuit or product.

[0058]   It will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined in the appended claims. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.